REMARKS/ARGUMENTS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested.

Claims 1-13 and 15-22 are pending in this application. Claims 1 and 15 are amended by the present response. The changes to the claims are believed to find support in the disclosure as originally filed and thus are not believed to raise a question of new matter.

In the outstanding Office Action, Claims 1-8, 12, 14 and 15-22 are rejected under 35 U.S.C. §102(e) as anticipated by Admitted Prior Art, herein "APA"; and Claims 9-11 were objected to as dependent upon a rejected base claim, but were noted as allowable if rewritten in independent form to include all of the limitations of their base claim and any intervening claims.

Initially, Applicants gratefully acknowledge the early indication of the allowable subject matter in Claims 9-11. However, since Applicants consider that Claim 1 as amended patentably defines over the cited art, Claims 9-11 have presently been maintained in dependent form.

Applicants respectfully traverse the rejection of Claims 1-8, 12, 14 and 15-22 under 35 U.S.C. §102(e) as anticipated by APA.

Claim 1 recites, in part,

> wherein the plurality of memory cell arrays are located independently of each other and have a plurality of cell array groups each of which includes two or more different memory cell arrays, a first Pass/Fail signal indicative of success or failure of an operation is outputted in accordance with each cell array group, and the semiconductor memory device includes a memory chip including all of the plurality of memory cell array groups (Emphasis added)

Claim 15 recites similar features.

The outstanding Action states on page 3, lines 9-10 that Figure 2 of the present invention anticipates the feature "the semiconductor memory device includes a memory chip

including all of the plurality of memory cell groups," recited in Claim 1. In other words, the outstanding Action is stating that upper array 0 and lower array 0 shown in Figure 2 is "a memory chip including all of the plurality of memory cell groups."

However, as is clear from Figure 2 the upper array 0 and the lower array 0 are found on ***different chips***. The upper array 0 is a memory cell array found on the chip of chip address 0 and the lower array 0 is a memory cell array found on the chip of chip address 1.

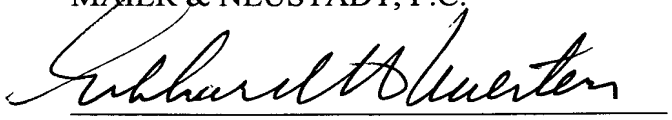
In contrast, Claims 1 and 15 recite that "the semiconductor memory device comprises ***a memory chip*** including all of the plurality of memory cell array groups" (emphasis added). As is shown in Figure 3 of the present application, a plurality of memory cell array groups are provided on a semiconductor device, which is on a single memory chip.

Accordingly as the APA does not teach or suggest all of the features recited in Claims 1 and 15, Applicants respectfully submit that Claims 1 and 15 and claims depending therefrom patentably distinguish over APA.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

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